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. 128 kn 128 dreams 128 crack 128 classic 128 bi 128. 192 zooming zm 18 zipper 18 zion 18 yuri 18 yorku 18 yorn 18. znk 11 zisfein 11 zeal 11 yugoslav 11 yuck 11 yorku 11Â .1. Field of the Invention The present invention relates to a drive circuit of a display panel, more particularly to a drive circuit capable of suppressing interference on data lines. 2. Description of the Related Art Referring to FIG. 1, a conventional drive circuit 10 includes a delay circuit 11, a source driver 13, a timing controller 15, and a display panel 17. The delay circuit 11 receives a picture signal DATA from a picture signal input terminal 1 for generating a plurality of shift signals SRH in response to the picture signal DATA. The source driver 13 is electrically connected to a plurality of data lines DL for driving data lines in response to the plurality of shift signals SRH. The

timing controller 15 is electrically connected to the source driver 13 for controlling the source driver 13 to generate a plurality of control signals ST in response to the plurality of shift signals SRH. A plurality of display pixels P of the display panel 17 are electrically connected to the plurality of data lines DL. The display pixels P are simultaneously display the data line data outputted from the source driver 13 in response to the plurality of control signals ST outputted from the timing controller 15. Conventionally, the picture signal DATA from the picture signal input terminal 1 contains the static picture data and the alternating current (AC) picture data. The static picture data represents the image of the display panel 17. The AC picture data represents a scanning pattern for sampling the static picture data. FIG. 2 illustrates waveform diagrams of the shift signals SRH from the delay circuit 11, the plurality of control signals ST from the timing controller 15, and the data line data from the source driver 13 during an alternating current (AC) scan. As shown in FIG. 2, the delay circuit 11 generates the plurality of shift signals SRH in response to the picture signal DATA. The timing controller 15 generates the plurality of control signals ST in response to the plurality of shift signals SRH

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DB-11-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4-V4-W4

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